REMARKS

Claims 1-12 are now presented for examination. Claim 12 has been amended strictly as to a matter of form. Claims 1, 6 and 12 are the only independent claims.

Claims 1-12 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 4,745,485 (Iwasaki). Applicants submit that independent Claims 1, 6 and 12 are patentable over the cited art for at least the following reasons.

Claim 1 recites a memory controller including a serial/parallel converter section for converting serial input data into parallel data, an FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the data read out from the frame memory section. Claim 6 recites a memory controller including a serial/parallel converter section for performing a serial/parallel conversion of converting a-bit (a being a positive integer) input data into axn-bit data, an FIFO memory section for temporarily storing converted axn-bit data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the axn-bit data read out from the

frame memory section. Claim 12 recites a liquid crystal display apparatus. The apparatus includes an interface for transforming various video signals and transmission signals standard video signals, a decoder for transforming standard video signals into video signals for displaying images on liquid crystal, a liquid crystal display panel, and a drive section for driving the display panel according to the video signals. The decoder includes a memory controller comprising a serial/parallel converter section for converting serial input data into parallel data, an FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the data read out from the frame memory section.

By virtue of the structure recited in the independent claims, there is no need for more than one frame memory. This advantageously reduces the cost of the device and simplifies the structure as compared to prior art devices, which require multiple frame memories. Since the frame memory can be a single frame memory, the data input and output can be made continuous.

On the other hand, Iwasaki, as understood by Applicants, shows a display device having multiple frame memories. Specifically, the picture element data is read out

from the frame memory 4 and displayed in the upper display area 11 and written in frame memory 5. Subsequently, the picture element data is read out from the frame memory 5, corresponding to the lower display area 12. Writing and reading of the frame memories 4 and 5, reading of the frame memory 4 and reading of the frame memory 5 are performed alternately.

That is, for devices such as that described in Iwasaki, it is indispensable for the device to have at least one pair of frame memories 4 and 5 to alternately perform reading and writing. This slows down writing speed and is expensive. Applicants note that this type of prior art system is described in the background section of the specification in relation to the conventional device shown in Figure 2. Accordingly, independent Claims 1, 6 and 12 are believed patentable over the cited art.

A review of the other art of record has failed to reveal anything which, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as a reference against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the

same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

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